Attached hereto is a marked-up version of the specification and claims 1-5, which illustrates all of the changes made to the specification and claims pursuant to 37 CFR §1.121. The attached page is captioned "**Version With Markings To Show Changes Made**". Deleted language is bracketed and added language is underlined.

The Commissioner is hereby authorized to charge any deficiencies or credit any overpayments in connection with the filing of this correspondence to Deposit Account No. **50-0426**.

Respectfully submitted,

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Version With Markings To Show Changes Made

IN THE SPECIFICATION:

The paragraph heading has been inserted on page 1 of the English translation of the subject application, before line 5, as follows:

Technical Field

The paragraph heading has been inserted on page 1 of the English translation of the subject application, before line 8, as follows:

Background Art

The paragraph heading has been inserted on page 2 of the English translation of the subject application, before line 4, as follows:

Summary of the Invention

The paragraph heading has been inserted on page 3 of the English translation of the subject application, before line 19, as follows:

Brief Description of the Drawings

The paragraph heading has been inserted on page 3 of the English translation of the subject application, before line 30, as follows:

Detailed Description of the Invention

IN THE CLAIMS:

The paragraph heading "Patent Claims" on page 8 of the English translation of the subject application has been deleted and the paragraph heading has been inserted in place thereof as follows:

CLAIMS

The paragraph heading has been inserted on page 8 of the English translation of the subject application, before claim 1, as follows:

What is claimed is:

1. (Amended) A circuit for generating an asynchronous signal pulse having a predetermined duration at an output of an integrated circuit, which has

a first and a second transistor [(2, 3)] in the integrated circuit, which are connected in series between a supply potential (U_{DD}) and ground (GND), firstly a control pulse [(A)] having the predetermined duration being present at a control connection [(G1)] of the first transistor [(2)] and then a control pulse [(B)] being present at a control connection [(G2)] of the second transistor [(3)], with the result that, for the predetermined duration, firstly the first transistor [(2)] and then the second transistor [(3)] is turned on and the connecting point [(4)] is firstly at the supply potential (U_{DD}) and then at the ground (GND), and

a resistor [(6, 7)] for the definition of the active signal state, which is connected outside the integrated circuit in parallel with one of the two transistors [(2, 3)] in the integrated circuit either between the supply potential (U_{DD}) and the

connecting point [(4)] or between the ground (GND) and the connecting point [(4].

2. (Amended) The circuit as claimed in claim 1, wherein a waiting time (Δt) is provided between the first control pulse [(A)] and the second control pulse [(B)], in which the two pulses do not overlap.

3. (Amended) The circuit as claimed in claim [1 or] 2, wherein one of the two control pulses [(B)] is generated from the other of the two control pulses [(A)] by an inverter delay device.

4. (Amended) The circuit as claimed in [one of the preceding claims] claim 1, wherein the first transistor [(2)] is a P-channel MOS transistor and the second transistor [(3)] is an N-channel MOS transistor, the control connection [(G1)] of the first transistor being inverted.

5. (Amended) The circuit as claimed in claim 4, wherein the first transistor [(2)] and the second transistor [(3)] form a CMOS inverter with independent control gate connections.